D. Remarks

Rejection of Claims 4 and 16-19 Under 35 U.S.C. §103(a), based on Applicants' Background Art (*Background Art*) in view of U.S. Patent No. 6,385,028 (*Kuono*).

The rejection of claim 4 will first be addressed.

Claim 4 depends from claim 1. Claim 1 includes the limitation of at least two clamping circuits corresponding to two IGFETs varying from one another.

To establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.

The combination of references does not show at least two clamping circuits that vary from one another. The rejection admits that the *Background Art* does not show such a limitation.[1] Such a limitation is not shown in *Kuono*, either.

Kuono is directed to a power MOSFET application, and so only shows a single power MOSFET[2]. That is, *Kuono* teaches the selection criteria for a single transistor, thus cannot show or suggest clamping circuits for two IGFETs.

Because the combination of references does not show or suggest two clamping circuits that vary from one another, this ground for rejection is traversed.

The rejection of claims 16-19 will now be addressed.

The invention of claim 16 is directed to a method for designing a protective circuit for a semiconductor integrated circuit device. The method includes executing a simulation with a predetermined charged device model (CDM) equivalent circuit. The CDM equivalent circuit includes a first clamping device, a first IGFET, and a second clamping device. The gate of the first IGFET is connected to an I/O terminal by a first resistance (Rin). The first and second clamping devices are connected to one another through a second resistance (Rg). The method further includes selecting a ratio (Rg/Rin) that prevents a potential between the gate and source/drain of IGFET from exceeding a predetermined value.

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[1] See the Office Action, dated 3/17/03, Page 3, Lines 17-18.

[2] See *Kuono* all figures, which only shows one power MOSFET transistor.

A charge device model (CDM) equivalent circuit is understood by those skilled in the art, and clearly defined in Applicants' Specification, which distinguishes the CDM model from the human body model (HBM) and machine model (MM):

> For appraisal according to HBM and MM models, electric charges can be applied between two predetermined terminals of a device. In contrast, for appraisal according to a CDM model, a package and a chip of the device can be charged with electricity. Such charge can then be discharged to an outside location through terminals of the device.[3]

It is admitted that the Applicants' *Background Art*, does not show the selection of the claimed ratio (Rg/Rin) based on a CDM model.[4] However, such a limitation is not shown or suggested by *Kuono* either.

Kuono is not related to CDM model, and teaches away from such an arrangement by showing only an MM or HBM type model. This is clearly shown by the FIG. 7 of *Kuono*, which is labeled "Simulation Model".[5] In the model shown, a charge (on capacitor C) is applied between two terminals of the device: the load terminal B+ and ground. Thus, the charge is applied between two predetermined terminals of the device, and addresses the MM or HBM type model. The charge does not originate from a package and a chip of the device, as included in the CDM model. *Kuono* therefore, teaches away from Applicants' arrangement by reinforcing HBM or MM type models, and remaining silent as to CDM models.

Thus, because it is admitted that the *Background Art* does not show the selection of a resistance ratio based on a CDM model simulation, and the other reference *Kuono* is unrelated to CDM models, the combination of references cannot show or suggest all limitations of Applicants' claim 16, and this ground of rejection is traversed.

Dependent claim 17 includes additional limitations not shown in the cited reference. Claim 17 recites that a predetermined potential value (between a gate and source/drain) is also determined from CDM test results and ratios Rg/Rin.

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[3] Applicants' Specification, Page 2, Lines 5-10, emphasis added.
[4] See the Office Action, dated 3/17/03, Page 2, last three lines.
[5] See *Kuono*, FIG. 7, and corresponding brief description of drawing at Col. 3, Line 17.

This rejection is traversed on two grounds. First, the rejection is traversed for the same essential reasons as set forth for claim 16. Namely, it is admitted that the *Background Art* does not show the selection of a resistance ratio based on a CDM model simulation, and *Kuono* is unrelated to CDM models.

Second, claim 17 recites the step of determining a predetermined potential value based on two criteria: the CDM test results and simulation results showing a relationship between a gate-source/drain potential and Applicants' ratio Rg/Rin. Both the *Background Art* and *Kuono* provide no teachings regarding the determination of such a "not to exceed" predetermined potential. In both cases, voltage between a gate and source-drain is simply applied over a range.[6]

Thus, because none of the reference relied upon shows or suggests the determination of a "not to exceed" predetermined potential based on any criteria, the limitations of claim 17 are not shown or suggested. Accordingly, the rejection of claim 17 is traversed on these additional grounds.

Claim 19 also includes limitations not shown or suggested by the cited reference. Claim 19 is directed to changing the properties of a second clamping device for a second IGFET in order to prevent a potential between terminals of a first IGFET from exceeding a predetermined value.

The *Background Art* does not teach changing the properties of a second clamping device of one IGFET to affect properties of another IGFET. In fact, the *Background Art* teaches away from such an arrangement by stressing utilization of same size CDM devices for all input/output terminals.[7] It is not possible for *Kuono* to show or suggest such a limitation, as *Kuono* is directed to a power MOSFET application with a single MOSFET.

Thus, because the references do not show or suggest all limitations of claim 18, and in fact teach away from such limitations, the rejection of claim 19 is traversed on these additional grounds.

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[6] See Applicants' Specification, FIG. 16, and discussion at Page 5, Lines 4-13, which applies a voltage Vox, but never determines a voltage based on any criteria. See also *Kuono*, FIG. 9, and discussion at Col. 9, Lines 25-28, which only applies a voltage. It is again emphasized, the example of *Kuono* is not a CDM model.

[7] See Applicants' Specification, Page 8, Lines 12-14.

Rejection of Claims 1-3, 7, 8, 10-13 15 and 20 Under 35 U.S.C. §103(a), based on the *Background Art* in view of U.S. Patent No. 5,515,226 (*Tailliet*).

The rejection of claims 1-3, 7, 8, 10-13 and 15 will first be addressed.

The semiconductor integrated circuit device of claim 1 includes a plurality of IGFETs coupled to a corresponding I/O terminal through a corresponding first resistance. A first clamping circuit is coupled to each I/O terminal. A second clamping circuit corresponds to each IGFET. Each second clamping circuit includes a second clamping device and the corresponding first resistance. Each second clamping device has a first terminal connected to a gate electrode of the corresponding IGFET and a second terminal connected to a source/drain terminal of the corresponding IGFET and a supply potential wiring. Each first clamping device is coupled to one second clamping device through a second resistance. At least two of the second clamping circuits vary from one another.

No Motivation for Proposed Combination

As noted above, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found in either the references themselves or in the knowledge generally available to one of ordinary skill in the art.

In Applicants' previous response to Office Action, grounds for traversing this rejection were set forth based on a lack of motivation to combine the references. In Applicants' argument, it was shown that the *Background Art* is directed to a charge device mode CDM model, while *Tailliet* was directed to HBM or MM models. Evidence in support of the argument was presented by citations to the references relied upon by the rejection. The argument remains unrebutted.[8]

Applicants' thus resubmit this argument with additional evidence. Differences between the CDM mode and HBM and MM models are set forth in Applicants' Specification, which shall be cited once again:

[8] See the Office Action, dated 3/17/03, Response to Argument spanning Pages 6 and 7. No response is presented to address Applicants' claims that there is no motivation to combine the references.

> For appraisal according to HBM and MM models, electric charges can be applied between two predetermined terminals of a device. In contrast, for appraisal according to a CDM model, a package and a chip of the device can be charged with electricity. Such charge can then be discharged to an outside location through terminals of the device.[9]

Like *Kuono*, *Tailliet* is only related to CDM model, and teaches away from such an arrangement by showing an MM or HBM type model. This is clearly shown by all teachings set forth in *Tailliet*.

The "Background and Summary of Invention" of *Tailliet* only describes an HBM or MM type model:

> FIG. 2 shows the simplest configuration generally used to protect a pad Pj connected by a conductor Cj to an input Ej... The input Ej... must be protected against electrostatic discharges.[10]

> The electrostatic discharges... are diverted towards the ground bus BM, thus preventing overvoltages from appearing at the conductor Cj and hence at the input Ej. The arrangement is the same for the other pads...[11]

Thus, the "Background and Summary of Invention" of *Tailliet* teaches the application of charge between two predetermined terminals of a device (Pad Pj and Pad P1), which is the HBM or MM mode, and not the CDM model.

The remainder of *Tailliet* is no different, and once more shows only an HBM or MM mode, and provides no teachings related to the CDM model:

> Indeed, the electrostatic discharge on the pad Pj causes the limiter EC1j to be placed in a state of conduction, shunting the discharge current towards the ground

[9] Applicants' Specification, Page 2, Lines 5-10, emphasis added.
[10] *Tailliet*, Col. 2, Lines 9-14.
[11] *Tailliet*, Col. 2, Lines 24-28.

BM and from there towards the ground pad P1...[12]

> The protection device according to the invention works as follows: when an electrostatic discharge reaches the access pad Pj, the first limiter EC1j becomes conductive... If the discharge current is equal to some amperes, a voltage drop of several volts (for example about 20 volts for a current of 4 amperes) may occur in the ground bus BM between the pad P1 and the pad Pj.[13]

Thus, the remainder of *Tailliet* teaches the application of charge between two predetermined terminals of a device (Pad Pj and Pad P1). Once again, this is the HBM or MM mode, and not the CDM model.

The above is believed to present conclusive evidence that *Tailliet* is unrelated to the CDM model, thus there would be no motivation to combine the HBM or MM model of *Tailliet* with the CDM model of the *Background Art*.

It is also well established that if a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.[14]

Applicants further traverse this rejection by noting the combining *Tailliet* with the *Background Art* would or render the *Background Art* unsuitable for its intended purpose. As noted above, *Tailliet* is directed to HBM or MM type models. Thus, combining *Tailliet* with the *Background Art*, would force the HBM or MM model teachings of *Tailliet* onto the CDM model teachings of the *Background Art*. Such an application of divergent models would change the principle operation of the *Background Art* to an HBM or MM protective device, rather than the CDM protective device.

All Limitations Not Shown or Suggested by Proposed Combination of the Rejection

Still further, the combination of references does not show all limitations of claim 1. As noted above, claim 1 recites second clamping circuits, each corresponding to a different IGFET, where at least two such clamping circuits vary from one another.

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[12] *Tailliet*, Col. 3, Lines 54-57.
[13] *Tailliet*, Col. 3, Lines 48-60.
[14] In re Gordon, 221 USPQ 1125 (Fed. Cir. 1984).

The rejection admits that the *Background Art* fails to show such a limitation.[15]

However, such a limitation is not shown in the other reference *Tailliet*, either. The rejection has presented various rationales for showing such a limitation. However, all such rationales are believed to be insufficient.

A first rationale was presented as follows:

> Tailliet discloses the second limiter (EC2j) of transistor (ELj) can be varied depending on the protection level needed by the transistor (ELj) due to its location relative to the pad which it is connected (see col. 3, lines 15-19).[16]

However, this cited portion of *Tailliet* does not show variation between two second limiters. The cited portion is set forth below, in full.

> A second limiter is not necessary for all the pads... it is possible to use only one limiter for those circuit elements needing protection that are geographically quite close to the pad... to which they are connected. The elements that are further away use a second limiter according to the invention. Furthermore, those circuit elements to be protected that are connected to pads which are themselves located sufficiently close to the pad to be protected could use only one limiter located in the peripheral part.[17]

It is clear from the above excerpt that this portion of *Tailliet* is directed to the inclusion or exclusion of a second limiter, not a variation between second limiter, as claimed.

A second rationale was presented as follows:

> Tailliet does teach that dimensions of the second clamping circuits (EC2j) will vary, depending on the values of the input resistor Rj (see Col. 4, Lines 43-47).[18]

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[15] See the Office Action, dated 3/17/03, Page 3, Lines 17-18.
[16] See the Office Action, dated 3/17/03, Page 3, Line 20 to Page 4, Line 1.
[17] *Tailliet*, Col. 3, Lines 10-18.
[18] See the Office Action, dated 3/17/03, Page 6, Line 21 to Page 7, Line 1.

This portion of *Tailliet* does not show variation between second limiters. The cited portion is set forth below, in full.

> However, if the input Ej is a field-effect transistor gate or another element with high input impedance, the value of the resistor Rj is not of critical importance. It will be chosen so as to be sufficiently high to limit the current in the second limiter EC2j to an acceptable value (that depends on the dimensions of the limiter EC2j).

It is clear from the above excerpt that this portion of *Tailliet* is directed to the selection of a resistor value Rj, and provides no suggestion for providing two different values for Rj, and thus establishing variation recited in claim 1.

A third rationale was presented as follows.

> In addition, the resistance of ground bus (BM) can vary according to the position of the input/output terminals (Pj). Therefore, variation of the (EC2j) arises due to differences of the wiring resistance of ground bus (BM) and the input terminal resistor (Rj).

This teaching is presented without reference to any portion of *Tailliet*. As such, the teaching is not taken from the cited art and cannot present a prima facie case of obviousness. A citation to *Tailliet* in support of this rejection is respectfully requested.

The above teaching is not believed to come from *Tailliet* as it contradicts express teachings from the reference. In particular, the statement "variation of the (EC2j) arises due to differences of the wiring resistance of ground bus (BM) and the input terminal resistor (Rj)" contradicts *Tailliet*. *Tailliet* teaches that a value Rj depends on the dimensions of the limiter EC2j. The rejection relies on the complete opposite: that EC2j will vary according to Rj.

Still further the above rationale states that "variation of the (EC2j) arises due to differences of the wiring resistance of ground bus (BM)". This teaching is not in the reference.[19]

[19] The reference has been reviewed in detail, and such a teaching cannot be found. Again, a citation is respectfully requested.

Accordingly, the reference *Tailliet* does not show variations between second clamping circuits, as recited in claim 1.

For all of these reasons, a prima facie case of obviousness has not been established for claim 1, and this ground of rejection is traversed.

Various claims depending from claim 1 are believed to include additional limitations not shown by the cited combination.

Claim 3 recites that at least two second clamping devices that vary by having second clamping circuits with different capabilities. Claim 15 recites second clamping devices with different construction.

As noted above, *Tailliet* provides no description of how one voltage limiter may or may not differ from another, let alone how such limiters can differ in capability. Thus, the combination of references is not believed to be suggestive of the limitations of claim 3 or 15, either.

Claim 8 recites that a majority of at least one first resistance includes non-wiring structures. This limitation was not addressed by the rejection.[20] Thus, the burden of prosecution cannot have been met for this claim, and the rejection is traversed.

Claim 12 adds the limitation that a second terminal of each second clamping device is connected to a second supply terminal different from a first supply terminal. To show such limitations, the rejection argues

> Tailliet discloses the first clamping circuit (EC1j) and second clamping circuit (EC2j) are connected to different power supply terminals (between Pj and P1, see fig. 3).[21]

However, P1 is not a power supply terminal, but an access pad, which sends or receives signals, not a power supply.[22] Also, if P1 is a power supply terminal, then *Tailliet* does not show an I/O terminal, and thus cannot show numerous limitations of independent claim 1.

Thus, because the combination does not show or suggest all limitations of claim 12, a

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[20] See the Office Action, dated 3/17/03, Page 4, Last two lines. There is no mention of the majority of at least one first resistance.
[21] See the Office Action, dated 3/17/03, Page 5, Lines 15-16.
[22] See *Tailliet*, Col. 1, Lines 41-46.

prima facie case of obviousness has not been established for this claim.

The rejection of claim 20 will now be addressed.

No arguments were presented regarding claim 20. Further, no arguments were presented regarding claims 16 or 19, from which claim 20 depends. As a result, the burden of prosecution cannot have been met for these claims, and this ground of rejection is traversed.

Rejection of Claims 5, 6 and 14 Under 35 U.S.C. §103(a), based on *Background Art* in view of *Tailliet*.

To the extent that this ground of rejection relies on the combination of the *Background Art* in view of *Tailliet*, Applicants' incorporate by reference herein the comments set forth above for claim 1.

Rejection of Claim 9 Under 35 U.S.C. §103(a), based on *Background Art* in view of *Tailliet*, and further in view of U.S. Patent No. 5,942,916 (*Matsbara et al.*).

To the extent that this ground of rejection relies on the combination of the *Background Art* in view of *Tailliet*, Applicants' incorporate by reference herein the comments set forth above for claim 1.

Claim 19 has been amended, not in response to the cited art, but to address a typographical error. The present claims 1-20 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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